

### REMARKS

The Final Aaction mailed December 13, 2005 has been carefully considered. Reconsideration and allowance of the subject application, as amended, are respectfully requested. Claims 1, 5, 8, 12, 14, 18, 20 and 24 have been amended to overcome the Examiner's formal rejections thereto, and to further define the invention over the art. No new matter has been added to the subject application as a result of the changes made thereto.

In particular, independent claims 1, 8, 14 and 20 have been amended to clarify that the clock speed is lowered from a first clock speed to a second clock speed based on the sleep message. As will be set forth below, Applicants respectfully submit that these amendments place the currently pending claims in condition for allowance.

Turning to the rejections on the art, claims 1, 8, 14, 20 and 26-29 stand rejected under 35 USC 103 as being unpatentable over Datta et al. in view of Gregorian et al. Applicants respectfully submit this rejection is in error.

In pertinent part, the Examiner points to Datta et al. as disclosing "logic [290, 390 similar] to selectively lower a speed of a clock signal from a first clock speed [bit\_clk131] to a second clock speed [cased] corresponding with the sleep state [col. 4, l. 51 – col.5, l. 17; clock speed corresponding with the sleep state is cessation]." (page 3, Final Action) The Examiner concedes that Datta does not discuss the concept of using different protocols (cipher 6, page 3, Final Action).

The Examiner points to Gregorian as disclosing a system for selectively lowering the clock speed of the clock from a first clock speed [e.g., F1] to a second speed {e.g. F2}, wherein the first clock speed controls the communication adapter [semiconductor chip] to communicate with a transmission medium according to a first communication protocol having a first data transmission rate [e.g., E3] and the second clock speed controls the communication adapter to communicate with the transmission medium according to a second communication protocol having a second data transmission rate [e.g., DS3] [cipher 7, page 3. Final Action). Applicants respectfully disagree with the Examiner's characterization of Gregorian.

Gregorian appears to disclose a method and apparatus for automatically determining the protocol being used from the frequency of an applied clock. The clock's frequency is identified when its frequency falls into the set range for which the apparatus is targeted. Based on the

detecting frequency in the set range, a mode select signal is generated. The mode select signal causes the chip to configure to the appropriate frequency for that mode, as well as any other unique configuration perimeters. (Summary of the Invention)

Thus, it appears that Gregorian is directed to determining the protocol based on the clock frequencies supplied to the chip. Importantly, the Examiner also asserts that Gregorian teaches “setup configuration that selectively lowers the speed of the clock to the associated protocol.” (cipher 7, page 3, Final Action). Applicants disagree. In contrast to the Examiner’s assertion, it does not appear that Gregorian teaches that the clock speed is lowered, rather, Gregorian teaches that the mode of operation of the semiconductor chip changes in response to the clock speed. Moreover, nowhere does Gregorian disclose or suggest the concept of changing between communication protocols based on a sleep message.

Returning to the Datta reference, Applicants agree with the Examiner that Datta discloses two states of operation: operating normally and complete cessation of the clock signal upon the occurrence of a sleep message. Thus, according to the teachings of Datta, when a sleep message is received it appears that no communication occurs since the clock is completely ceased (stopped).

Accordingly, if one were to combine the teachings of Gregorian with the teachings of Datta, one would be left with two states of operation: an operative state where the system is running without a sleep message and a state where the system is not operating when the sleep message occurs (i.e. cessation). Thus, it is not entirely understood why the examiner is combining Gregorian with Datta, since it appears that the combined teachings of these two references would not yield a result that reads on Applicants’ invention of the independent claims.

In contrast, Applicants’ invention of independent claim 1 requires “logic to selectively lower a speed of a clock signal from a first clock speed to a second clock speed based on the sleep message, the first clock speed controls the communication adapter to communicate with a transmission medium according to a first communication protocol having a first data transmission rate and the second clock speed controls the communication adapter to communicate with the transmission medium according to a second communication protocol having a second data transmission rate” (claim 1). Applicants’ invention of independent claims 8, 14 and 20 each require similar limitations.

Thus, it is respectfully submitted that since nowhere does Gregorian disclose or suggest the concept of lowering the speed of a clock signal from a first clock speed to a second clock speed based on a sleep message, and Datta only discloses a normal operating mode and sleep mode (where in sleep mode all activity is stopped since the clock signal is ceased), it is respectfully submitted that no combination of Datta and Gregorian et al. could achieve or render obvious Applicants' invention of independent claims 1, 8, 14 and 20, and thus, it is respectfully submitted that the Examiner's rejection of these claims, and all claims dependent thereon, is in error and should be withdrawn.

Claims 4-5, 11-12, 17-18 and 23-24 stand rejected under 35 USC § 103 as being unpatentable over Datta and Gregorian as applied to claim 1 above, and further in view of Huang et al. Applicants respectfully submit this rejection is also in error.

The deficiencies of Datta and Gregorian vis-à-vis Applicants' invention of independent claim 1 is discussed above in detail. It is not seen how Huang supplies the missing teachings to Datta or Gregorian to achieve or render obvious Applicants' claimed invention.

The Examiner relies on Huang as teaching a system that comprises logic to determine the speed of the clock signal in response to a message and logic to selectively lower the speed of a clock signal if the speed of the clock signal exceeds a predetermined clock speed.

Claims 4-5, 11-12, 17-18 and 23-25 each depend directly or indirectly from Applicants' invention of independent claims 1, 8, 14 or 20, as the case may be, and thus, must be read as incorporating the limitations of the independent claim. 35 USC §112, 4<sup>th</sup> paragraph. In summary, no combination of Datta, Gregorian and Huang disclose or suggest that the speed of a clock signal is lowered from a first clock speed to a second clock speed based on a sleep message. Thus, it is respectfully submitted that the Examiner's rejection of claims 4-5, 11-12, 17-18 and 23-24 under 35 USC §103 as being unpatentable over Datta and Gregorian, in view of Huang, is in error and should be withdrawn.

Claims 6, 13, 19 and 25 stand rejected under 35 USC §103 as being unpatentable over Datta and Gregorian as applied to claim 1 above, and further in view of Foster. Applicants respectfully submit this rejection is also in error. The Examiner relies on Foster as disclosing a system for placing a communication adapter in an auto-sensing state in response to a resume message.

Claims 6, 13, 19 and 25 each depend directly or indirectly from Applicants' invention of independent claims 1, 8, 14 or 20, as the case may be, and thus, must be read as incorporating the limitations of these claims. 35 USC §112, 4<sup>th</sup> paragraph. Suffice to note that nowhere does the combination of Datta, Gregorian and Foster disclose or suggest selectively lowering the speed of a clock from a first clock speed to a second clock speed based on a sleep message.

Finally, claim 7 stands rejected under 35 USC §103 as being unpatentable over Datta and Gregorian as applied to claim 1 above, and further in view of Greszczuk. Applicants respectfully submit this rejection is also in error.

The Examiner relies on Greszczuk as disclosing a system that comprises a data bus coupled between the communication adapter and the processing system, and wherein the processing system further comprises logic to selectively initiate a write command on the data bus addressed to the communication adapter specifying a change in one of a power state in response to a sleep message.

Claim 7 depends directly from Applicants' invention of independent claim 1 and thus must be read as incorporating the limitations of claim 1. 35 USC §112, 4<sup>th</sup> paragraph.

Moreover, no combination of Datta, Gregorian and Greszczuk disclose or suggest selectively lowering a speed of a clock signal from a first clock speed to a second clock speed based on a sleep message. Accordingly, it is respectfully submitted that the Examiner's rejection of claim 7 as being unpatentable over Datta and Gregorian in view of Greszczuk is in error and should be withdrawn.

Having dealt with all the objections raised by the Examiner, it is respectfully submitted that the present application, as amended, is in condition for allowance. Thus, early allowance is earnestly solicited.

If the Examiner desires personal contact for further disposition of this case, the Examiner is invited to call the undersigned Attorney at 603.668.6560.

In the event there are any fees due, please charge them to our Deposit Account No. 50-2121.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.116  
Serial Number: 10/005,969  
Filing Date: November 6, 2001  
Title: Communication Adapter  
Assignee: Intel Corporation

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Dkt: P12804 (INTEL)

Respectfully submitted,

SOUBHI ABDULKARIM

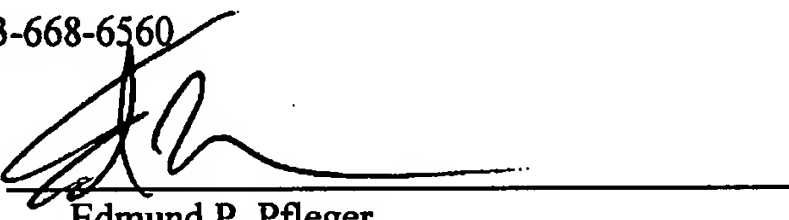
By his Representatives,

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603-668-6560

Date 2/13/06

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 13 day of February, 2006.

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